offsetting a first [said] pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and

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offsetting said first [said] pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

6. A system of displaying digital video data comprising pixel values [using pulse width modulation], comprising:

a logic circuit offsetting a first [said] pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and

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display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

REMARKS

This application was originally filed on June 2, 1998 with ten claims, two of which were written in independent form. No claims have been allowed. Claims 1 and 6 have been amended by this amendment for the purpose of more clearly reciting the claimed invention, not to distinguish the claims from the prior art.

Claims 1 and 6 were objected to because the preamble stated "pulse width modulation" while Claims 1 and 6 recited "offsetting a first pixel . . . pixel value" were not described in the preamble. The applicant respectfully submits that it is not completely clear what the Examiner is objecting to. The applicant knows of no requirement to describe each element of the claims in the preamble. Claims 1 and 6 have been amended to delete the reference to pulse width modulation from the preambles.

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Ishibashi et al.,

U.S. Patent No. 4,742,558 (Ishibashi). The applicant respectfully disagrees. Claim 1 recites, "offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value." The Examiner has not attempted to show where Ishibashi shows, teaches, or suggests, these limitations.

Claims 2, 3, and 5 were rejected under 35 U.S.C. § 102(b) as being anticipated by Ishibashi. The applicant respectfully disagrees. Claims 2, 3, and 5 depend from Claim 1 and should be deemed allowable for that reason and on their own merits.

Claim 6 was rejected under 35 U.S.C. § 102(b) as being anticipated by Ishibashi. The applicant respectfully disagrees. Claim 6 recites, "a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value." The Examiner has not attempted to show where Ishibashi shows, teaches, or suggests, these limitations.

Claims 7, 8, and 10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Ishibashi. The applicant respectfully disagrees. Claims 7, 8, and 10 depend from Claim 6 and should be deemed allowable for that reason and on their own merits.

Claims 4 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishibashi in view of Guttag et al., U.S. Patent 5,309,551 (Guttag). The applicant respectfully disagrees. The Examiner stated "Ishibashi teaches all of the claimed limitation with exception of the claimed bit map." The applicant respectfully submits that Claims 4 and 9 recite weighted bit-planes, not a bit map. Furthermore, the Examiner has not provided any suggestion in the prior art of record that would lead one of ordinary skill in the art to combine the two reference,

much less to combine and modify the two reference to achieve the recited invention. Claims 4 and 9 depend from independent Claims 1 and 6 and should be deemed allowable for that reason and on their own merits.

In view of the amendments and the remarks presented herewith, it is believed that the claims currently in the application, Claims 1-10, accord with the requirements of 35 U.S.C. § 112 and are allowable over the prior art of record. Therefore, it is urged that Claims 1-10 are in condition for allowance. Reconsideration of the present application is respectfully requested.

Respectfully submitted,

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